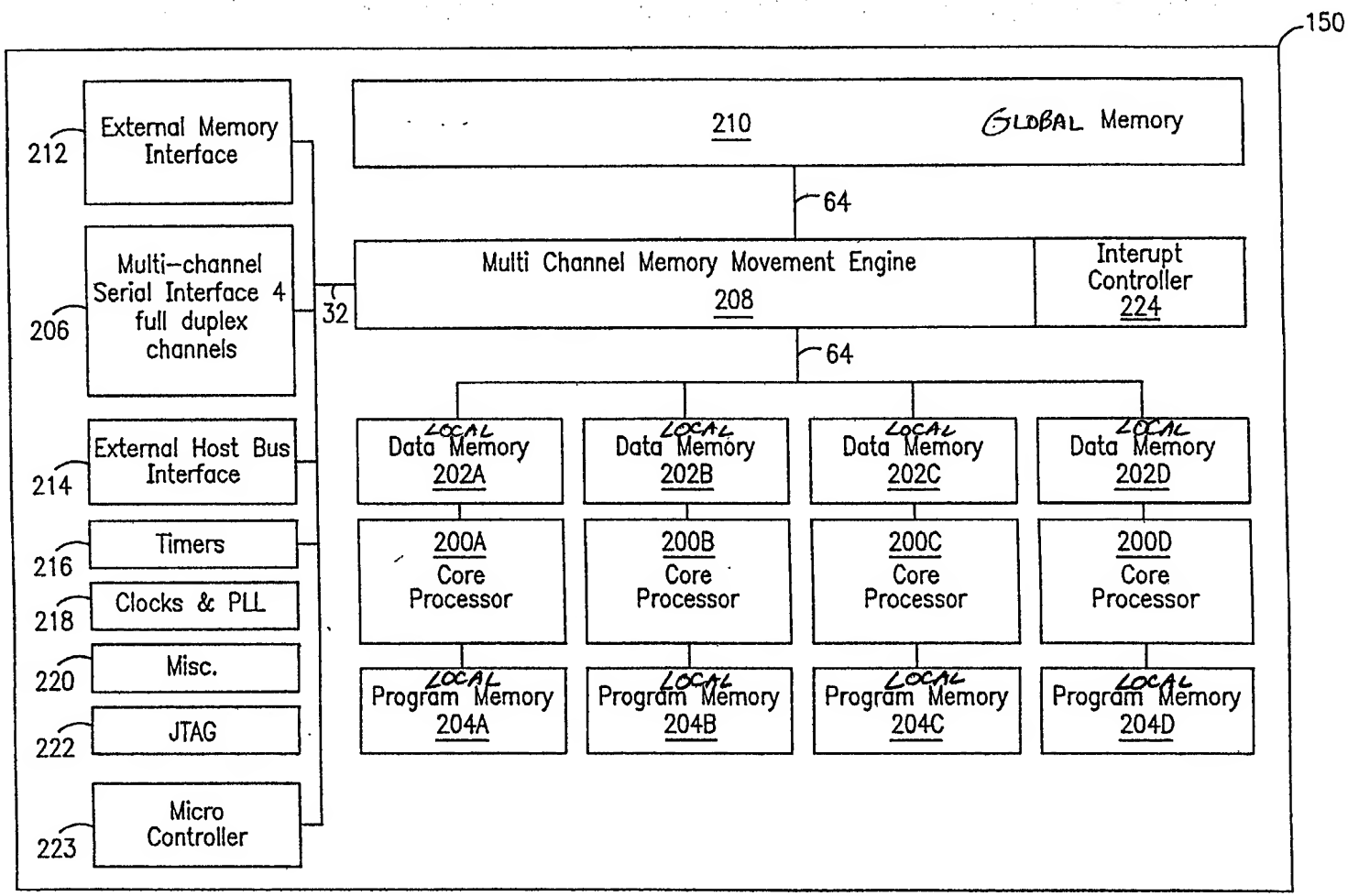

FIG. 1

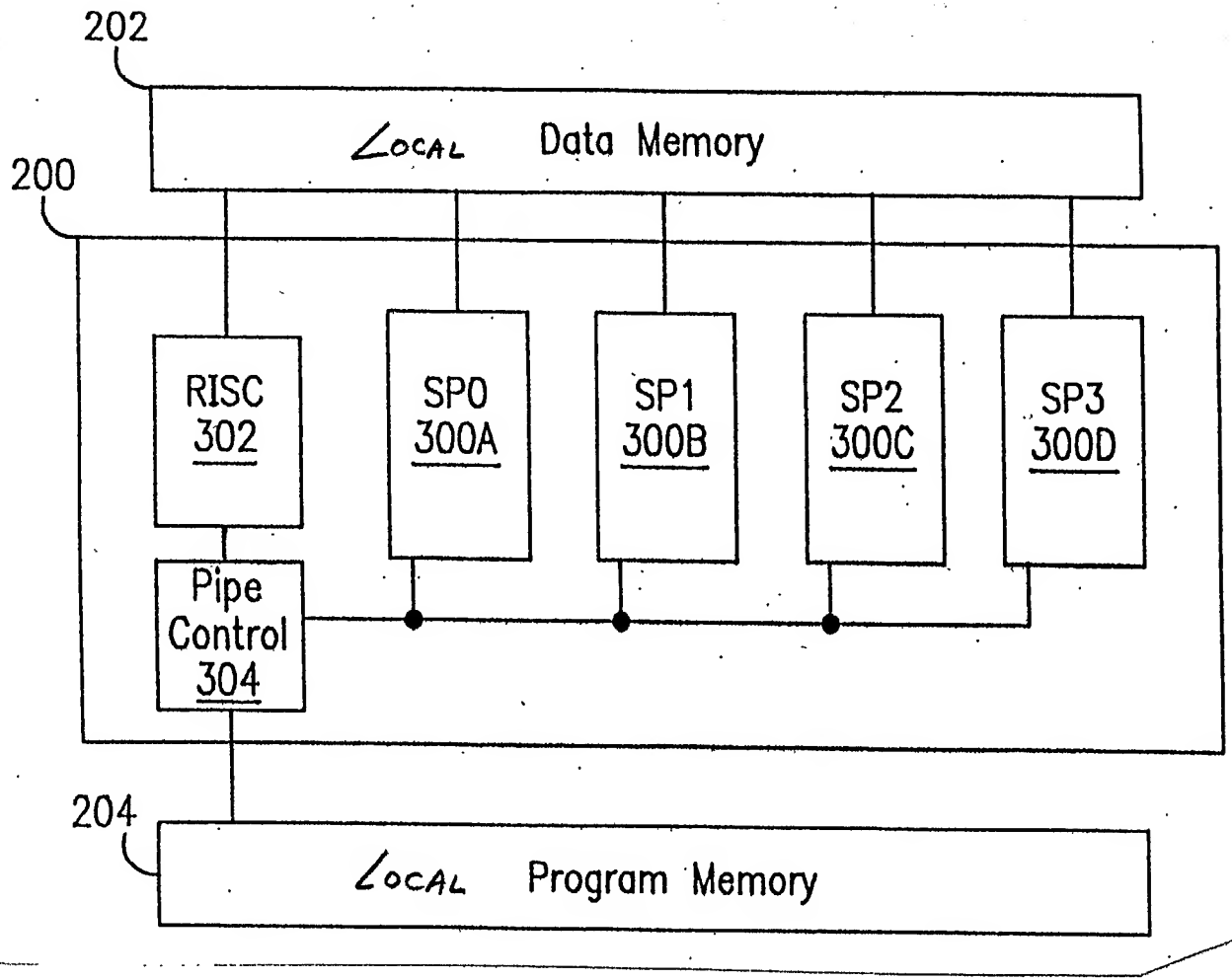

FIG. 2

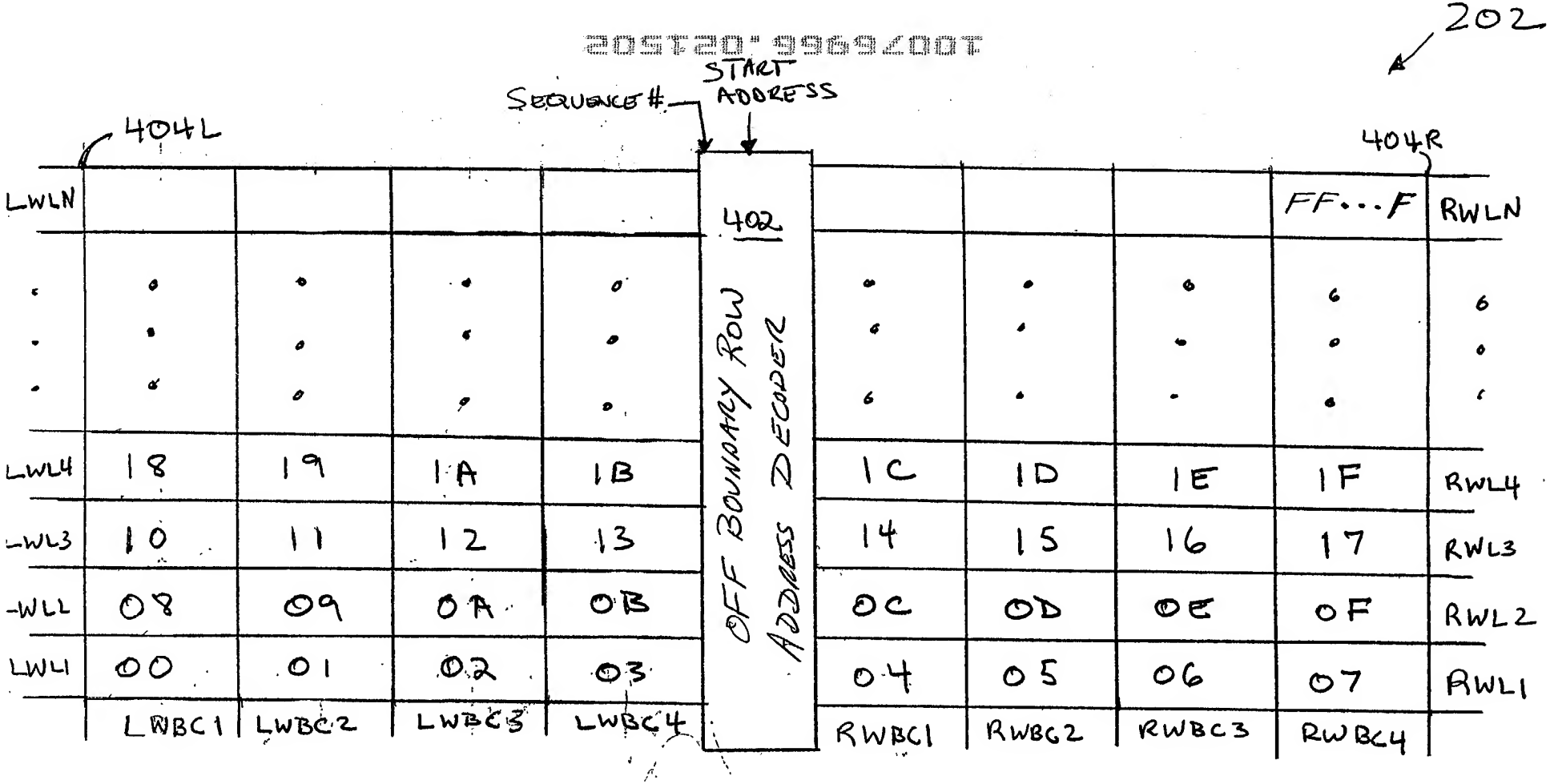
202
SEQUENCE #
START ADDRESS
404L
404R
402
OFF BOUNDARY ROW ADDRESS DECODER
LWLN
RWLN
FF...F
LWL4
RWL4
1 8
1 9
1 A
1 B
1 C
1 D
1 E
1 F
LWL3
RWL3
1 0
1 1
1 2
1 3
1 4
1 5
1 6
1 7
LWL2
RWL2
0 8
0 9
0 A
0 B
0 C
0 D
0 E
0 F
LWL1
RWL1
0 0
0 1
0 2
0 3
0 4
0 5
0 6
0 7
LWBC1
LWBC2
LWBC3
LWBC4
RWBC1
RWBC2
RWBC3
RWBC4

FIG. 3A

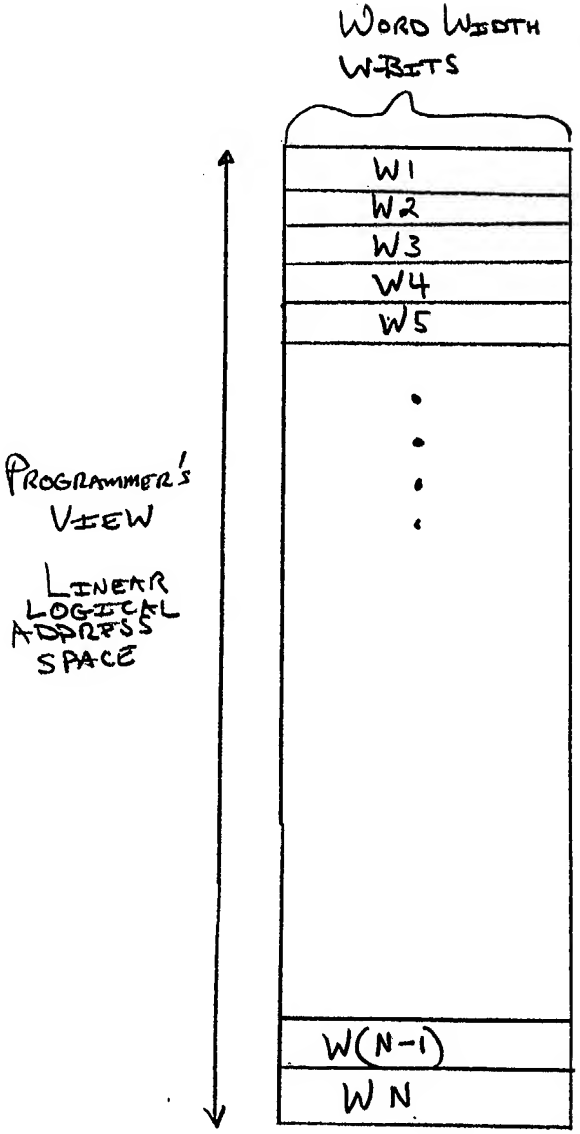
WORD WIDTH
W-BITS
W1
W2
W3
W4
W5
W(N-1)
W N
PROGRAMMER'S VIEW
LINEAR LOGICAL ADDRESS SPACE

FIG. 3B

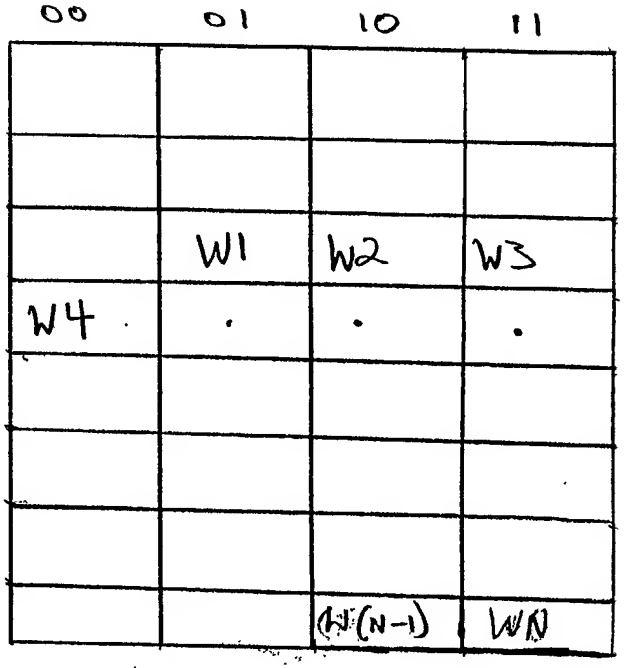
00
01
10
11
W1
W2
W3
W4
W(N-1)
WN
HARDWARE DESIGNER'S VIEW
OFFSET PHYSICAL ADDRESS SPACE

FIG. 3C

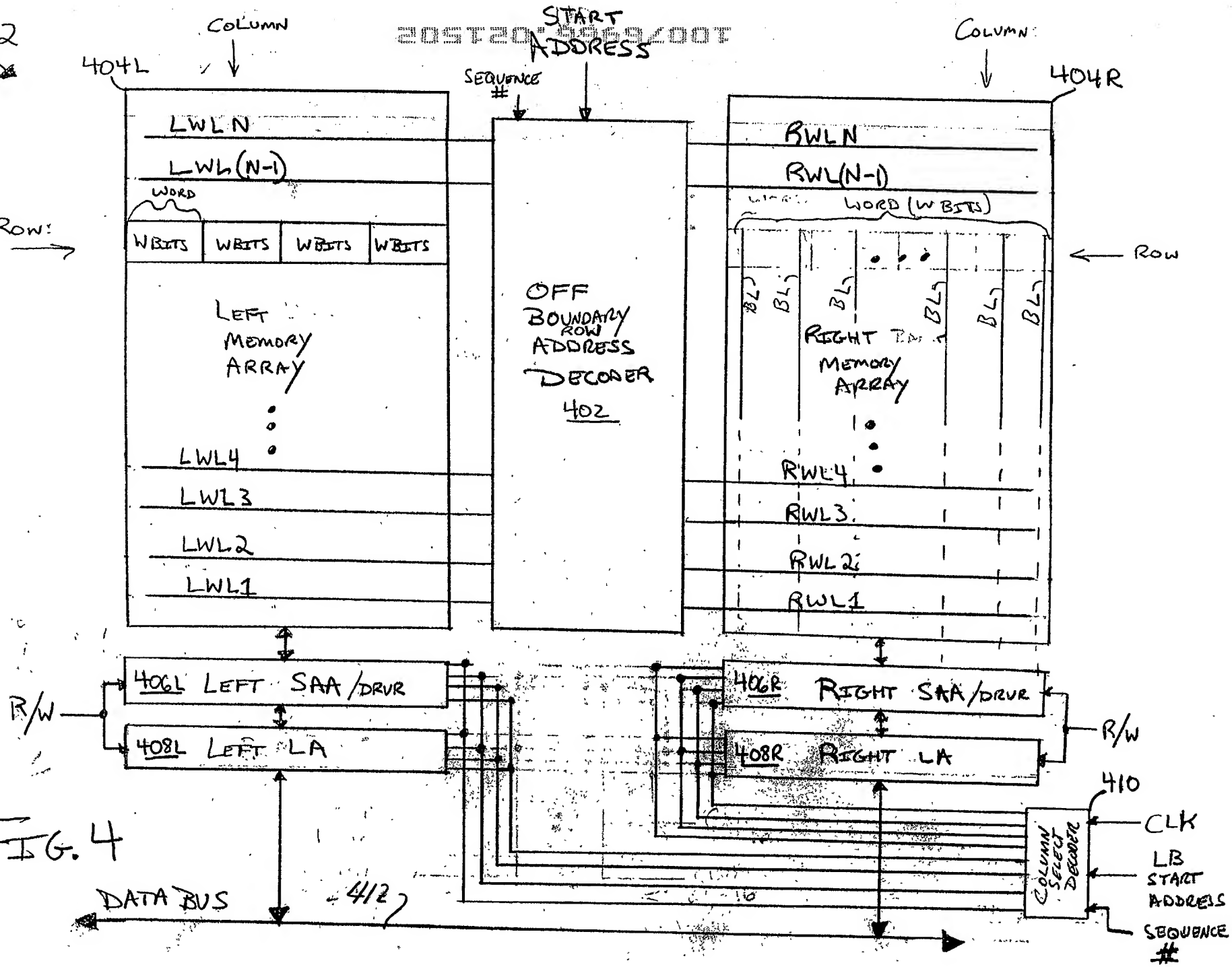
202
COLUMN
404L
START ADDRESS
SEQUENCE #
COLUMN
404R
LWLN
LWL(N-1)
WORD
WBITS
WBITS
WBITS
WBITS
ROW
LEFT MEMORY ARRAY
LWL4
LWL3
LWL2
LWL1
OFF BOUNDARY ROW ADDRESS DECODER 402
RWLN
RWL(N-1)
WORD (W BITS)
ROW
BL
RIGHT MEMORY ARRAY
RWL4
RWL3
RWL2
RWL1
406L LEFT SAA/DRVR
406R RIGHT SAA/DRVR
R/W
408L LEFT LA
408R RIGHT LA
R/W
410
CLK
LB START ADDRESS
SEQUENCE #
COLUMN SELECT DECODER
DATA BUS
412

FIG. 4

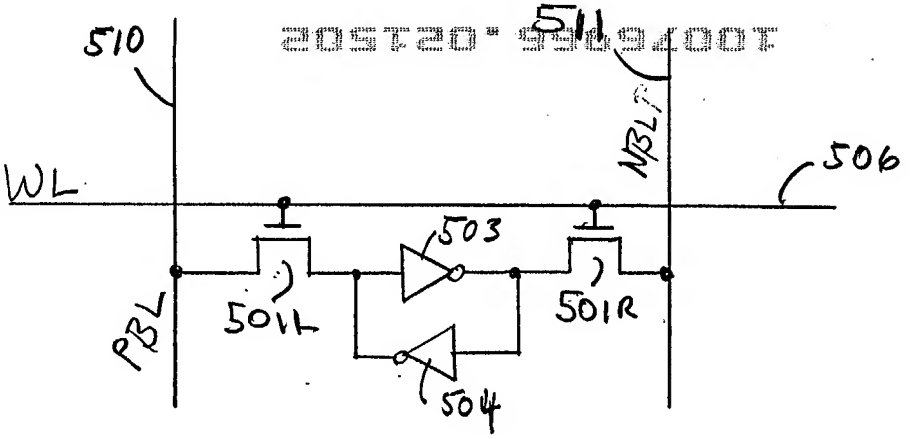

FIG. 5A

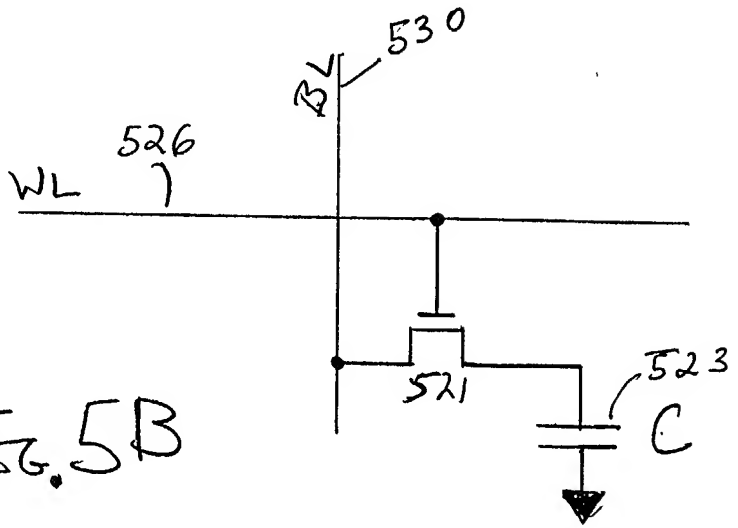

FIG. 5B

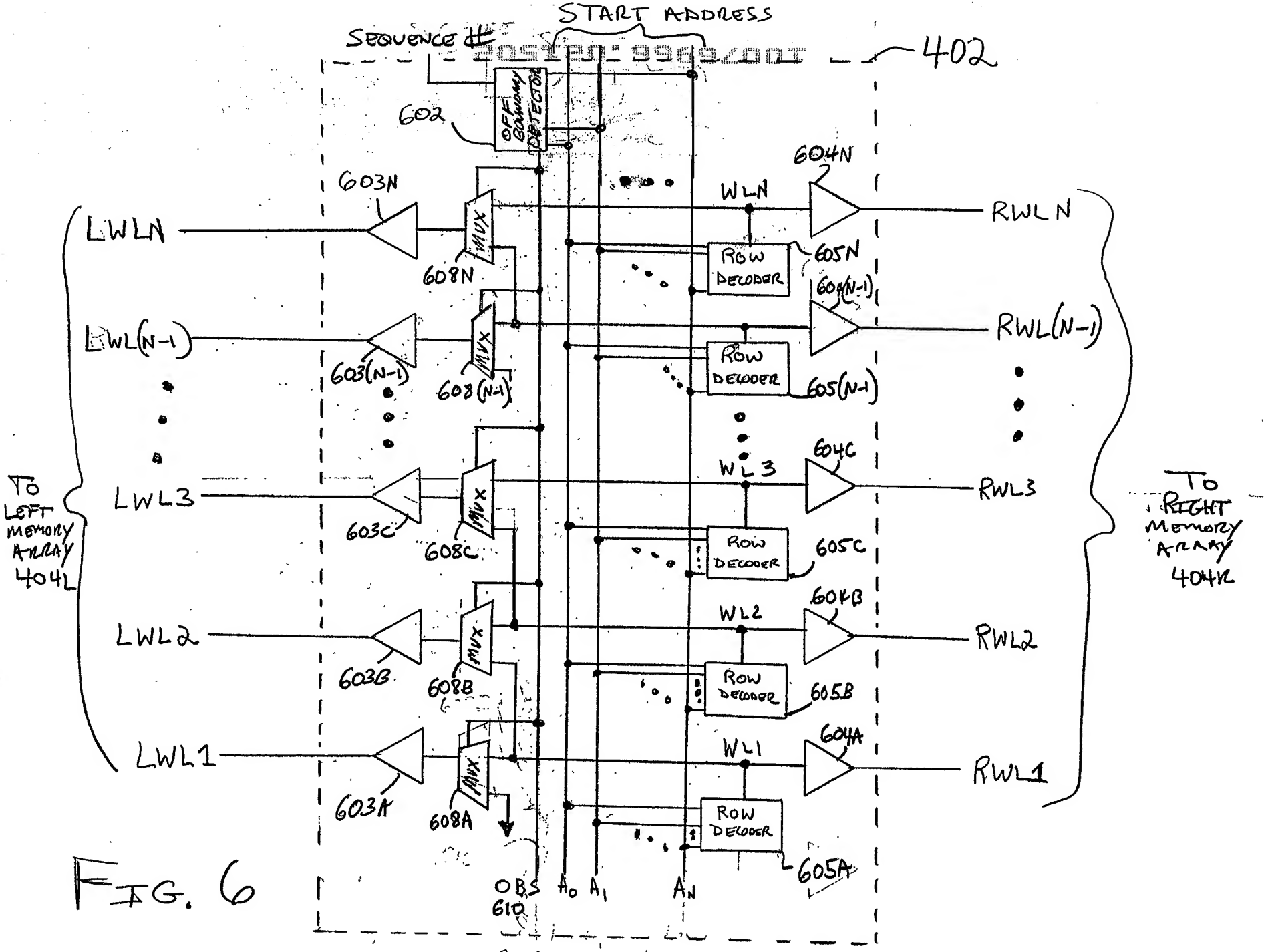
SEQUENCE #
START ADDRESS
402
602
OFF GAMMA DETECTOR
603N
608N
MUX
LWLN
WLN
604N
RWLN
ROW DECODER
605N
LWL(N-1)
603(N-1)
608(N-1)
604(N-1)
RWL(N-1)
605(N-1)
LWL3
603C
608C
WL3
604C
RWL3
605C
LWL2
603B
608B
WL2
604B
RWL2
605B
LWL1
603A
608A
WL1
604A
RWL1
605A
TO LEFT MEMORY ARRAY 404L
TO RIGHT MEMORY ARRAY 404R
OBS 610
A0
A1
AN

FIG. 6